Terma Case Study — Final Report

AAU, Terma

May 1, 2004

AMETIST DELIVERABLE 3.2.4

1 Introduction

This is the final AMETIST deliverable for task 3.2. on the Case Study 2: Memory Management in Radar Sensor Equipment. The case study has been provided by the partner Terma A/S who is developing and producing (amongst other things) radar sensor equipment typically used in areas were high performance is needed (monitoring of ground movement in airports, coastal surveillance, etc). The radar transceivers of Terma have a wide range of video processing facilities and in this case study the purpose is to model, analyze and synthesize the scheduling of memory access of two of these processing facilities. We refer to [1, 2] for a complete specification of the case study.

2 Summary of the work

During the first year of AMETIST all aspects of the case study was dealt with in substantial detail, including:

- An encoding of the existing scheduler in the BDD-based verification tool visualSTATE allowing correctness to be verified partially [1, 2].
- A sequence of encodings of the existing scheduler in UPPAAL leading to a complete verification of the correctness of the existing scheduler. Given the size of this model (21 timed automata and 20 integer variables) the verification time (less than 1 minute on a regular PC) is encouraging[1]. An initial UPPAAL model can be found in [5].
- Design of an optimal scheduler with respect to required size of buffers. This (general) design was obtained from experiments with an SMV model of a down-scaled scenario [6].

These results were presented to the hardware engineers at Terma in April 2003 with very positive response from the company and with suggested directions for further treatment. Thus, during the second year we have

- provided an extension of the UPPAAL model detailing the initialization and in particular the SDRAM structure[2]. This model was discussed with Terma A/S on the AMETIST meeting in September 2003 and found to be quite compatible with the VHDL design[3].

During the final year of AMETIST we have finally succeeded in

- *automatically* synthesizing the optimal schedule in terms of required buffer-size from [6] directly using the UPPAAL models [4, 3]. This work was carried out by Juhan Ernits, Tallin, during a Marie Curie Fellowship at BRICS autumn 2003 and finished during 2004. The method is based on an interesting (simple and efficient) synthesis method applying bit-state-hashing.

3 Conclusions

Concluding on the case study, we notice that the techniques and tools developed during AMETIST have been successfully used to *verify* the existing design provided by TERMA and *synthesize* optimal solutions to the scheduling problem, that would allow TERMA to completely eliminate the current large buffers used in the design and replace the current logic to dynamically arbitrate between many channels with a small precomputed fixed schedule. Although the system described in this case study is no longer under development, and thus direct application of our solutions are unlikely, we are confident that our approach could be applied to similar designs.

[1] The model can be downloaded from `http://www.cs.auc.dk/~kgl/Terma/terma-tsh.xml` and `http://www.cs.auc.dk/~kgl/Terma/terma-tsh.q`.

[2] See `http://www.cs.auc.dk/~kgl/Terma/terma-banks.xml` and `http://www.cs.auc.dk/~kgl/Terma/terma-banks.q`.

[3] See `http://ametist.cs.utwente.nl/RESEARCH/AALBORG/GERD/VP3_STHArbitrationindex.htm`

References

[1] G. Behrmann, S. Bernicot, T. Hune, K.G. Larsen, S. Lecamp, and A. Skou, *Case study 2: Memory interface for radar system*, 2002, Deliverable 3.2.1 from the IST project AMETIST.

[2] S. Bernicot and S. Lecamp, *Modelling and analysis a memory interface*, Master's thesis, University of Aalborg, 2002, Internal document from the IST project AMETIST.

[3] Juhan Ernits, *Abstraction based analysis and arbiter synthesis: Radar memory interface card case study revised*, Proceedings of Nordic Workshop on Programming Theory 2004, 2004.

[4] ———, *Memory arbiter synthesis and verification for a radar memory interface card*, Nordic Journal of Computing (2005), To appear5.

[5] E. Sasnauskaite and M. Mikucionis, *Memory interface analysis using the real-time model checker UPPAAL*, Master's thesis, University of Aalborg, 2002, Internal document from the IST project AMETIST.

[6] Gera Weiss, *Optimal Scheduler for a Memory Card*, Research report, Weizmann, 2002.