Terma Case Study — Second Year Report

AAU, Terma

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1 Introduction & Summary

This is the AMETIST second year deliverable for the task 3.2. on the Case Study 2: Memory Management in Radar Sensor Equipment. The case study has been provided by the partner Terma A/S who is developing and producing (amongst other things) radar sensor equipment typically used in areas were high performance is needed (monitoring of ground movement in airports, costal surveillance, etc). The radar tranceivers of Terma have a wide range of video processing facilities and in this case study the purpose is to model, analyse and synthesize the scheduling of memory access of two of these processing facilities. We refer to [1, 2] for a complete specification of the case study.

During the first year of AMETIST all aspects of the case study was dealt with in substantial detail, including:

- An encoding of the existing scheduler in the BDD-based verification tool visualSTATE allowing correctness to be verified partially.
- A sequence of encodings of the existing scheduler in UPPAAL leading to a complete verification of the correctness of the existing scheduler. Given the size of this model (21 timed automata and 20 integer variables) the verification time (less than 1 minute on a regular PC) is incouraging[1].
- Design of an optimal scheduler with respect to required size of buffers. This (general) design was obtained from experiments with an SMV model of a down-scaled scenario.

These results were presented to the hardware engineers at Terma in April 2003 with very positive response from the company. For future treatment of the case study the following directions were suggested:

- Analysis of the correctness of the existing scheduler taking more details wrt. the system initialization into account.
- Analysis of the correcntess of the existing scheduler taking more details wrt. the organization of the used SDRAM into account. The SDRAM is organised in four banks of equal size. Each bank is organised into rows and columns. A row must be activated before use. There can only be one active row per bank. A bank must be precharged (closed) before another row can be activated. There are several restrictions on when and how fast certain commands can be issued which should be reflected in our models.
- Investigage a systematic way for automatic translation of the VHDL designs used within the company into verification models.
- Possible application and examination of the flexibility our methodology on new designs to be provided by Terma A/S as a follow-up case study.

During the second year we have provided an extension of the UPPAAL model detailing the initialization and in particular the SDRAM structure[2]. This model was discussed with Terma A/S on the AMETIST meeting in September 2003 and found to be quite compatible with the VHDL design[3].

Application of our methodology on new designs is still a possibility but is awaiting the right project within the company.

As for the final year of AMETIST we plan the following:

[1] The model can be uploaded from `www.cs.auc.dk/~kgl/Terma/terma-tsh.{xml,q}`.
[2] See `www.cs.auc.dk/~kgl/Terma/terma-bank.{xml,q}`.
[3] See `http://ametist.cs.utwente.nl/RESEARCH/AALBORG/GERD/VP3_STHArbitrationindex.htm`

- Compile the UPPAAL modelling and verifications efforts on the original as well as the detailed models into a methodology report.
- Attempt to *automatically* synthesize the (buffer-size) optimal schedule from [3] using the UPPAAL models. Preliminary work carried out by Juhan Ernits, Tallin, a visiting Marie Curie Fellow at BRICS during the autumn of 2003 suggests a very interesting (simple and efficient) synthesis method applying bit-state-hashing.

References

[1] G. Behrmann, S. Bernicot, T. Hune, K.G. Larsen, S. Lecamp, and A. Skou. Case study 2: Memory interface for radar system, 2002. Available from World Wide Web: `http://www.cs.auc.dk/~kgl/AMETIST/bbhlls.ps`. Deliverable 3.2.1 from the IST project AMETIST.

[2] S. Bernicot and S. Lecamp. *Modelling and analysis a memory interface*. Master's thesis, University of Aalborg, 2002. Available from World Wide Web: `http://www.cs.auc.dk/~kgl/AMETIST/bl.ps`. Internal document from the IST project AMETIST.

[3] Gera Weiss. Optimal Scheduler for a Memory Card. Research report, Weizmann, 2002. Available from World Wide Web: `http://ametist.cs.utwente.nl/INTERNAL/PUBLICATIONS/WISPublications/Optimal_Schedule_for_a_Memory_Card`.