Terma Case Study

Deliverable 3.2.2

Terma A/S
Aalborg
Weizmann
Marseille

Overview

- Presentation of Case Study 2
- Overview of models and other contributions
- Meeting with Terma A/S
- Conclusions and future work

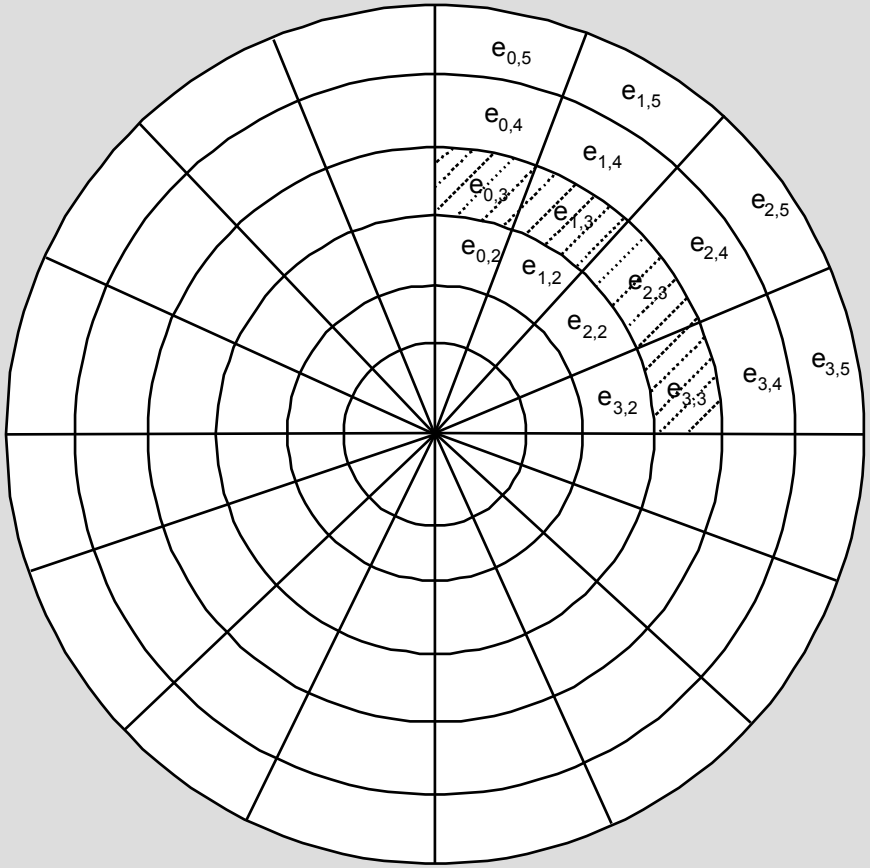
Case Study 2

- Provided by Terma A/S

  Terma is the leading contractor in Denmark within a host of defense related applications, such as army air defense, naval command and control, airborne electronic warfare, airborne tactical reconnaissance, aerial surveillance, ground based communication, and many more.

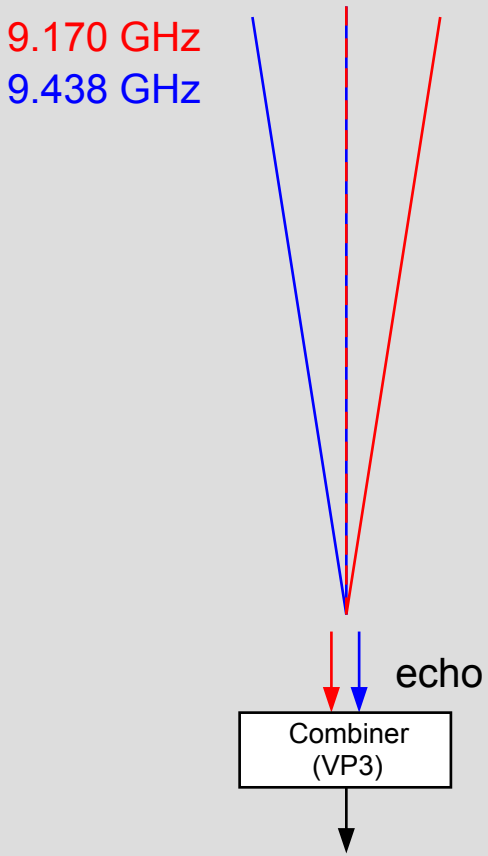
- Case study focuses on scheduling memory access in the video processing board of a radar system.

Sweep Integration



- A sweep is the data collected from a radius.
- Typical angle between sweeps is 0.036 degrees.
- Sweep integration sums over related cells from multiple sweeps.

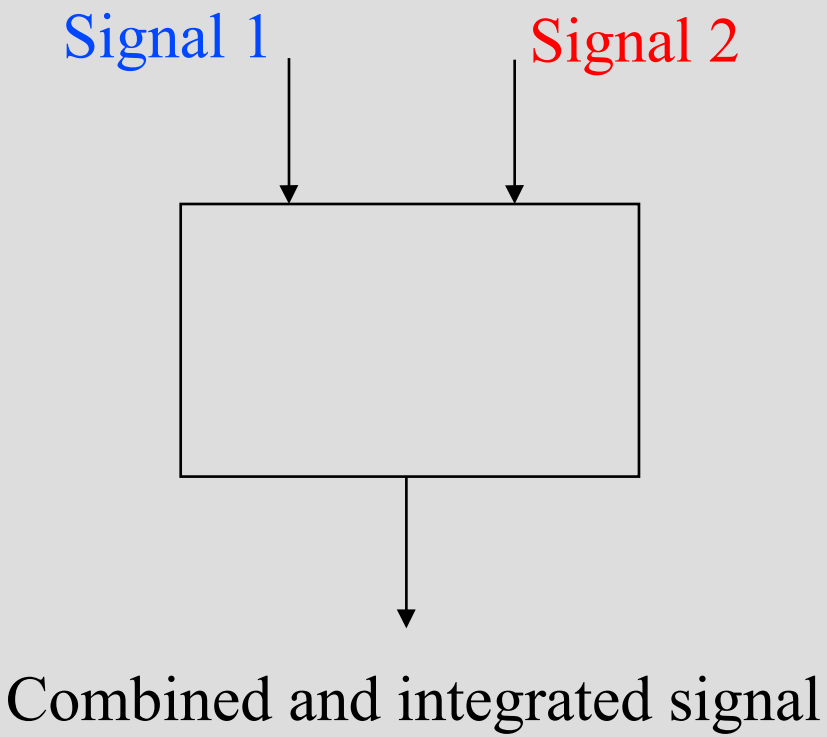
Frequency Diversity



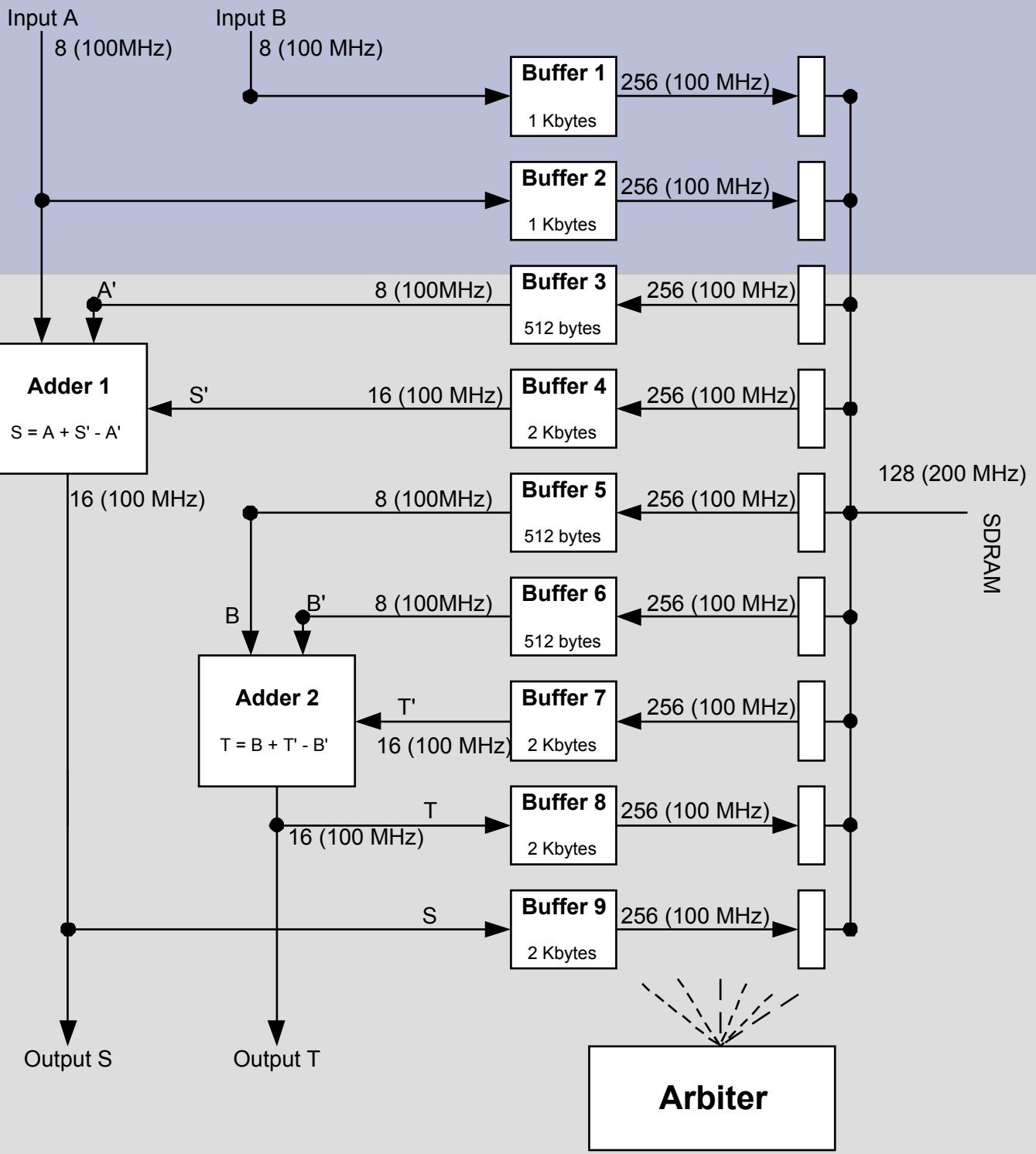
- Increased power
- Time delay between returns
- Different frequencies

- Removes noise

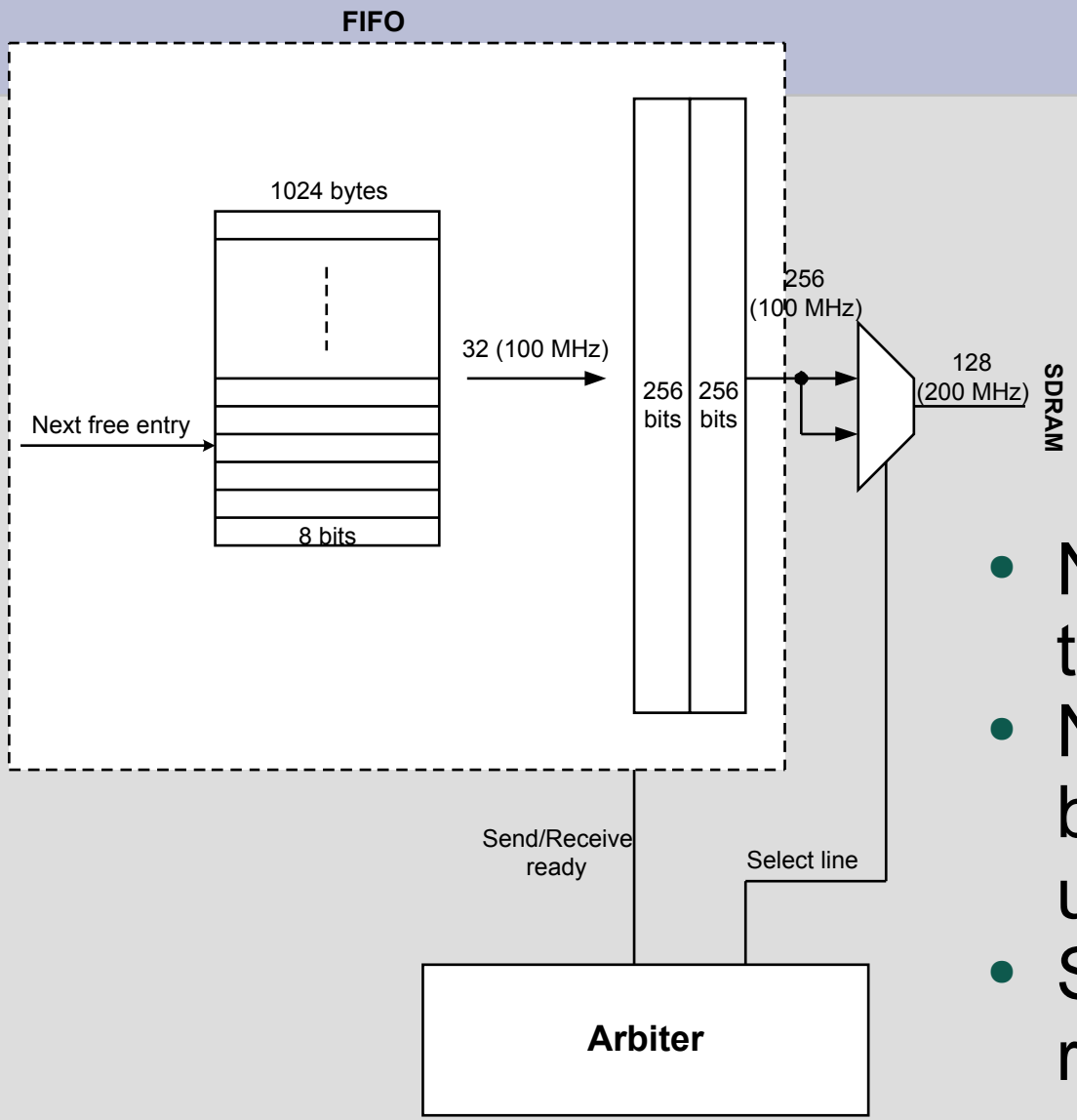
Video Processing Board



- Performs sweep integration
- Synchronizes the two signals by delaying signal 2
- Both tasks require that data is buffered


Input A
8 (100MHz)
Input B
8 (100 MHz)
Buffer 1
1 Kbytes
256 (100 MHz)
Buffer 2
1 Kbytes
256 (100 MHz)
A'
8 (100MHz)
Buffer 3
512 bytes
256 (100 MHz)
Adder 1
S = A + S' - A'
S'
16 (100 MHz)
Buffer 4
2 Kbytes
256 (100 MHz)
128 (200 MHz)
SDRAM
16 (100 MHz)
8 (100MHz)
Buffer 5
512 bytes
256 (100 MHz)
B
B'
8 (100MHz)
Buffer 6
512 bytes
256 (100 MHz)
Adder 2
T = B + T' - B'
T'
16 (100 MHz)
Buffer 7
2 Kbytes
256 (100 MHz)
T
16 (100 MHz)
Buffer 8
2 Kbytes
256 (100 MHz)
S
Buffer 9
2 Kbytes
256 (100 MHz)
Output S
Output T
Arbiter

A Single Buffer



- No runtime locking of the buffers!
- No runtime check for buffer overflows or underflows!
- SDRAM needs to be refreshed periodically.

Objectives

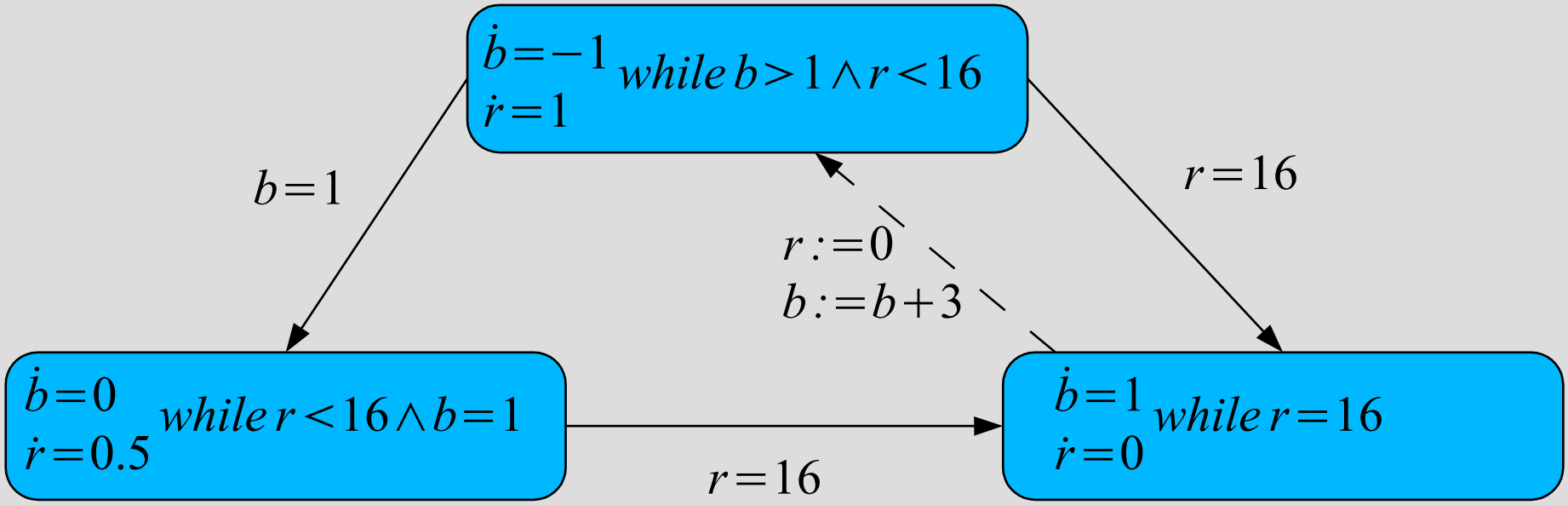
- Verify that overflow and underflow never happen
- Find minimum buffer size
- Synthesize better scheduling algorithm for the arbiter (better = smaller buffers)

Contributions

- Description of CS2 (Deliverable 3.2.1)
  [wrong link on the web-site]
- Models (Deliverable 3.2.2)
  [mistakenly called 4.2.2 in the deliverable]
  - VisualSTATE model (Bernicot, Lecamp)
  - Two timed automata model (Seshauskaire, Mikucionis, Behrmann)
  - SMV model (Gera Weiss)
  - Hybrid automata model (Gera Weiss)
  - SPIN model (Arne Skou)
- Provably optimal schedule (Gera Weiss)

Demo of TA Model

Hybrid Automata Model



r is the number of 32 bit elements in the register
b is the number of 16 bit elements in the buffer

Meeting with Terma

- Presentation of models
- Very positive feedback from Terma engineers
- New meeting at end of August:
  - Terma will present a new design of the next generation of the video processing board.
  - Terma might provide some of the VHDL design to us: opportunity for model extraction.

Conclusions and Future Work

- Very good progress:
  - 6 different models in 5 modeling formalisms
  - All models show that the current buffers are way to large
  - Optimal schedule found
- Terma is impressed by the progress so far
- Refine the model of the SDRAM
- Apply techniques to new design of video processing board
- Extract model from VHDL design
- Can we synthesize the optimal schedule?